



PRELIMINARY

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DS3890 BTL™ Octal Trapezoidal Driver

DS3892 BTL Octal TRI-STATE® Receiver

DS3898 BTL Octal Trapezoidal Repeater

General Description

The DS3890, DS3892 and DS3898 are advanced IEEE-896 Future Bus compatible devices designed specifically to overcome problems associated with driving densely populated backplanes. These products provide significant improvement in both speed and data integrity in comparison to conventional bus drivers and receivers. Their low output capacitance, low voltage swing and noise immunity features make them ideal for driving low impedance busses with minimum power dissipation.

The DS3890 and DS3898 feature open collector outputs that generate precise trapezoidal waveforms with typical rise and fall times of 6 ns which are relatively independent of capacitive loading conditions. These controlled output characteristics significantly reduce noise coupling to adjacent lines.

To minimize bus loading, the DS3890 and DS3898 also feature a schottky diode in series with the open collector outputs that isolates the driver output capacitance in the disabled state. With this type of configuration the output low

voltage is typically "1V". The output high level is intended to be 2 volts. This is achieved by terminating the bus with a pull up resistor. Both devices can drive an equivalent DC load of 18.5Ω (or greater) in the defined configuration.

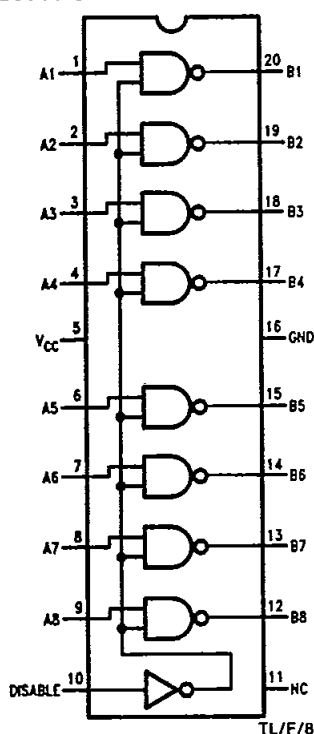
(General Description to be continued)

Features

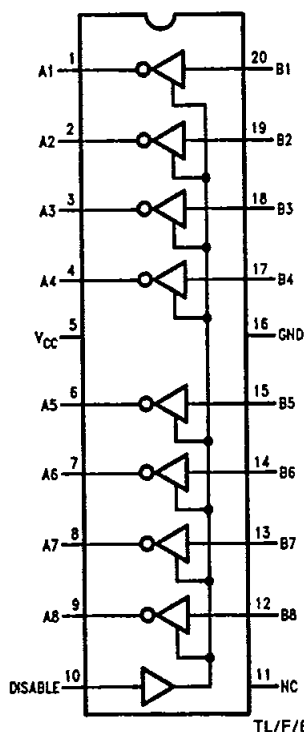
- Meets IEEE 896 Future Bus Specification
- Driver output capacitance less than 5 pF
- 1 volt bus signal reduces power consumption
- Trapezoidal driver waveforms (t_r , t_f , typically 6 ns) reduces noise coupling to adjacent lines
- Precise receiver threshold track the bus logic high level to maximize noise immunity in both logic high and low states
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection
- TTL compatible driver and control inputs and receiver output

Logic and Connection Diagrams

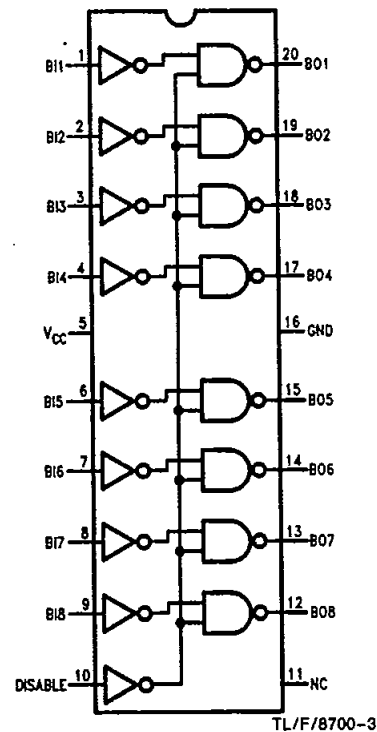
DS3890 Octal Future Bus Drivers



DS3892 Octal Future Bus Receivers



DS3898 Octal Future Bus Repeaters



Order Numbers DS3890J, N, DS3892J, N or DS3898J, N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Storage Temperature Range	-65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Temperature (T _A)	0	70	°C

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DS3890 Electrical Characteristics (Notes 2 and 3)**DRIVER AND CONTROL INPUTS**

Symbol	Conditions	Min	Typ	Max	Units
V _{IH}		2.0			V
V _{IL}				0.8	V
I _{IL} An	V _{CC} = Max V _{IN} = 0.4V		-1	-1.6	mA
I _{IL} Dis	V _{CC} = Max V _{IN} = 0.4V		-180	-400	μA
I _{IH}	V _{CC} = Max V _{IN} = 2.4V			40	μA
I _I	V _{CC} = Max V _{IN} = 5.25V			1	mA
V _{CL}	V _{CC} = Min I _{IN} = -12 mA		-0.9	-1.5	V

DRIVER OUTPUT

V _{OL}	V _{CC} = Min R _L = 18.5Ω	0.75	1.0	1.2	V
I _{OH}	V _{CC} = Max V _{OUT} = 2V	-20	10	100	μA
I _O	V _{CC} = 0V V _{OUT} = 2V			100	μA
I _{IL}	V _{CC} = Max V _{OUT} = 0.75V		-100	-250	μA
I _{CC} Low	V _{CC} = Max		50	80	mA
I _{CC} High				TBD	mA

DS3892 Electrical Characteristics (Notes 2 and 3)**CONTROL INPUTS**

Symbol	Conditions	Min	Typ	Max	Units
V _{IH}		2.0			V
V _{IL}				0.8	V
I _{IL}	V _{CC} = Max V _{IN} = 0.4V		-180	-400	μA
I _{IH}	V _{CC} = Max V _{IN} = 2.4V			40	μA
I _I	V _{CC} = Max V _{IN} = 5.25V			1	mA
V _{CL}	V _{CC} = Min I _{IN} = -12 mA		-0.9	-1.5	V

RECEIVER

V _{OL}	V _{CC} = Min I _{OL} = 16 mA		0.35	0.5	V
V _{OH}	V _{CC} = Min I _{OH} = -400 μA	2.4	3.2		V
I _{OS}	V _{CC} = Max V _{OUT} = 0V	-40	-70	-100	mA
V _{TH} Rec	V _{CC} = 5V	1.5	1.55	1.6	V
I _{IH} Rec	V _{CC} = Max V _{IN} = 2V		10	100	μA
I _I Rec	V _{CC} = 0V V _{IN} = 2V			100	μA
I _{IL} Rec	V _{CC} = Max V _{IN} = 0.75V			TBD	μA
I _{CC} Low	V _{CC} = Max			80	mA
I _{CC} High				TBD	mA

DS3898 Electrical Characteristics (Notes 2 and 3)

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CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	$V_{CC} = \text{Max}$ $V_{IN} = 0.4\text{V}$		-180	-400	μA
I_{IH}	$V_{CC} = \text{Max}$ $V_{IN} = 2.4\text{V}$			40	μA
I_I	$V_{CC} = \text{Max}$ $V_{IN} = 5.25\text{V}$			1	mA
V_{CL}	$V_{CC} = \text{Min}$ $I_{IN} = -12\text{mA}$		-0.9	-1.5	V

RECEIVER INPUT

$V_{TH \text{ Rec}}$	$V_{CC} = 5\text{V}$	1.5	1.55	1.6	V
$I_{IH \text{ Rec}}$	$V_{CC} = \text{Max}$ $V_{IN} = 2\text{V}$		10	100	μA
$I_I \text{ Rec}$	$V_{CC} = 0\text{V}$ $V_{IN} = 2\text{V}$			100	μA
$I_{IL \text{ Rec}}$	$V_{CC} = \text{Max}$ $V_{IN} = 0.75\text{V}$			TBD	μA

DRIVER OUTPUT

V_{OL}	$V_{CC} = \text{Min}$ $R_L = 18.5\Omega$	0.75	1.0	1.2	V
I_{OH}	$V_{CC} = \text{Max}$ $V_{OUT} = 2\text{V}$	-20	10	100	μA
I_O	$V_{CC} = 0\text{V}$ $V_{OUT} = 2\text{V}$			100	μA
I_{IL}	$V_{CC} = \text{Max}$ $V_{OUT} = 0.75\text{V}$		-100	-250	mA
$I_{CC \text{ Low}}$	$V_{CC} = \text{Max}$		90	135	mA
$I_{CC \text{ High}}$				TBD	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis and apply to the full operating temperature and V_{CC} range.

Note 3: All typical values are $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

DS3890 Switching Characteristics (Figure 1)

($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ unless otherwise specified)

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	An to Bn		9	15	ns
T_{dHL}			9	15	ns
T_{dLH}	Dis to Bn		10	18	ns
T_{dHL}			12	20	ns
$T_r \text{ \& } T_f$	Bn rise and fall time	3	6	10	ns

DS3892 Switching Characteristics (Figures 2, 3 and 4)

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bn to An		12	18	ns
T_{pHL}			10	18	ns
T_{dLZ}	Dis to An		10	18	ns
T_{dZL}			8	15	ns
T_{dHZ}			4	8	ns
T_{dZH}			7	12	ns
TNR	Receiver noise rejection	3	6		ns

DS3898 Switching Characteristics (Figures 4 and 5)

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Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bi to BOn		20	30	ns
T_{dHL}			20	30	ns
T_{dLH}	Dis to BOn		10	18	ns
T_{dHL}			12	20	ns
T_r & T_f	Bn rise and fall time	3	6	10	ns
TNR	Receiver noise rejection	3	6		ns

DS3890/DS3892/DS3898

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General Descriptions (Continued)

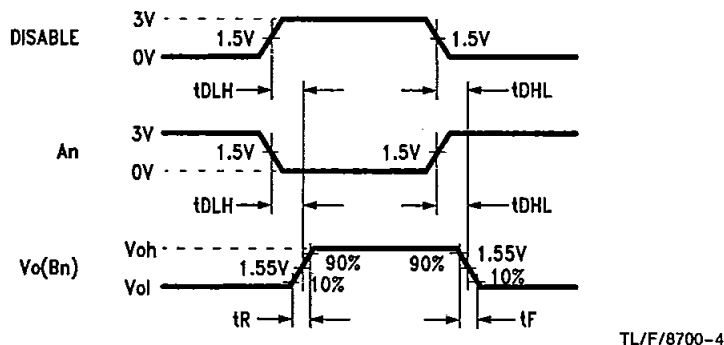
The DS8982 and DS3898 receiver inputs incorporate a low pass filter in conjunction with high speed comparator to further enhance the noise immunity. Both devices provide equal rejection to both positive and negative noise pulses (typically 6 ns) on the bus.

The DS3890 features TTL compatible inputs while both the DS3892 and DS3898 inputs are BTL compatible. The control inputs on all devices are TTL compatible.

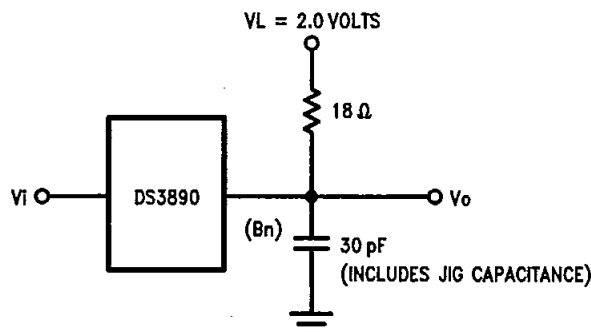
BTL "Backplane Transceiver Logic" is a new logic signaling method developed by IEEE P896 Future Bus Stan-

dards Committee. This standard was adopted to enhance the performance of Backplane Busses. BTL compatible bus interface circuits feature low capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard overcomes some of the fundamental limitations of TTL bus transceivers in heavily loaded backplane bus applications. Devices designed to this standard provide significant improvements in switching speed and data integrity.

AC Switching Waveforms



TL/F/8700-4



Note: $t_R = t_F < 10$ ns from 10% to 90%

TL/F/8700-5

FIGURE 1
Driver Propagation Delays

AC Switching Waveforms (Continued)

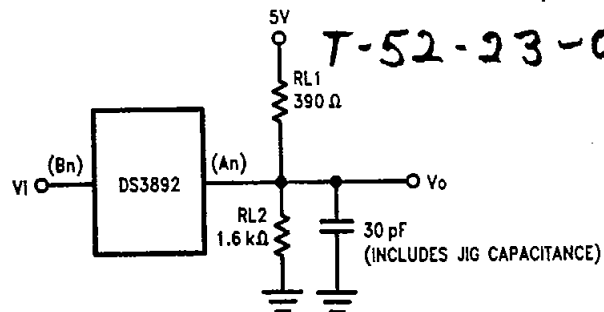
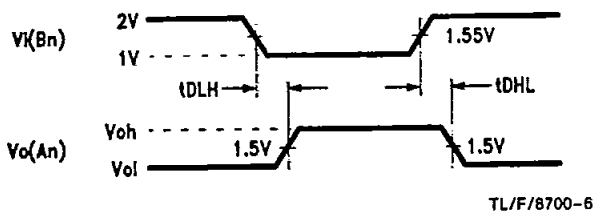
Note: $t_R = t_F < 10$ ns from 10% to 90%

FIGURE 2. Receiver Propagation Delays

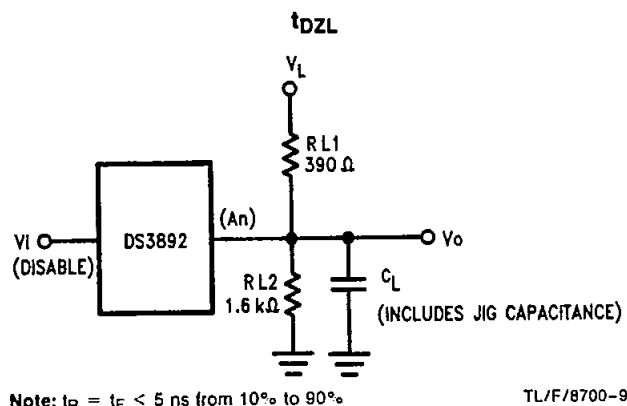
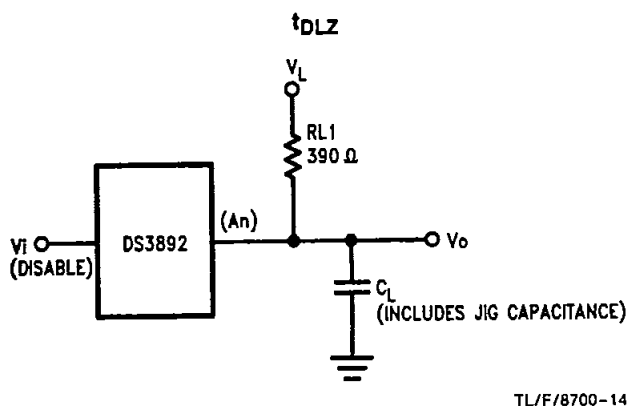
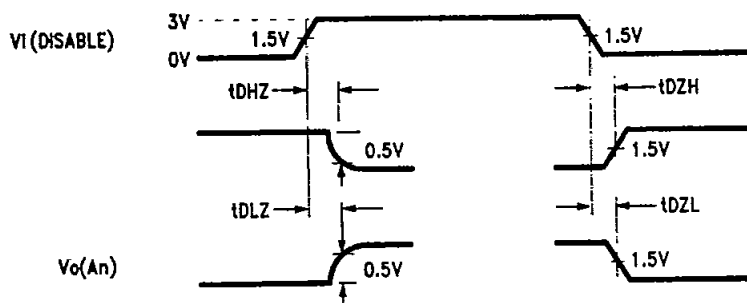
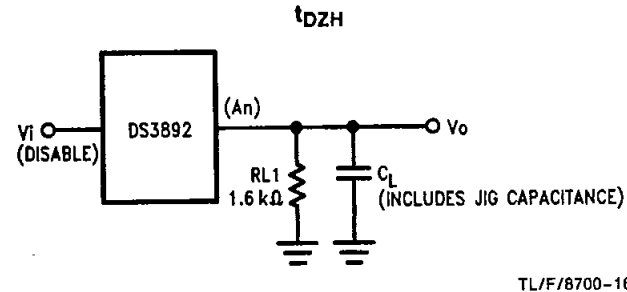
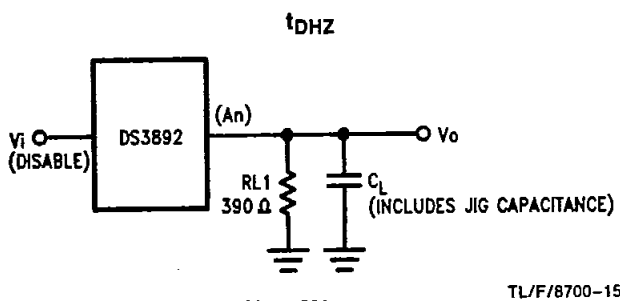
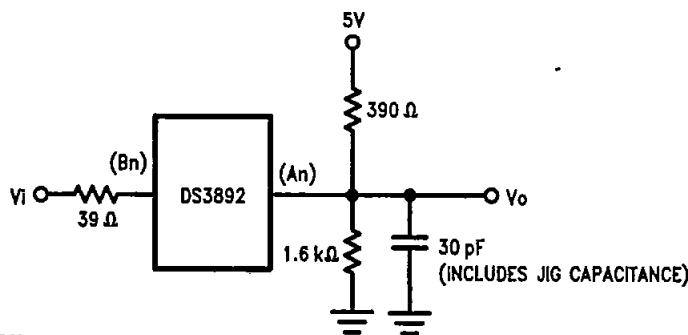
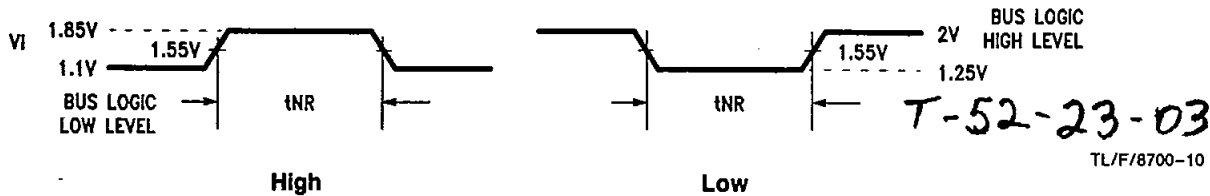
Note: $t_R = t_F < 5$ ns from 10% to 90%Note: $t_R = t_F < 5$ ns from 10% to 90%

FIGURE 3. Propagation Delay from Disable Pin to An

AC Switching Waveforms (Continued)

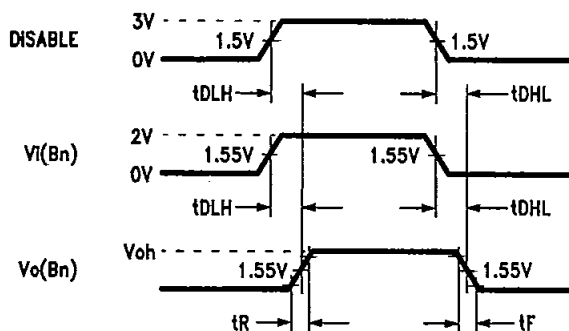
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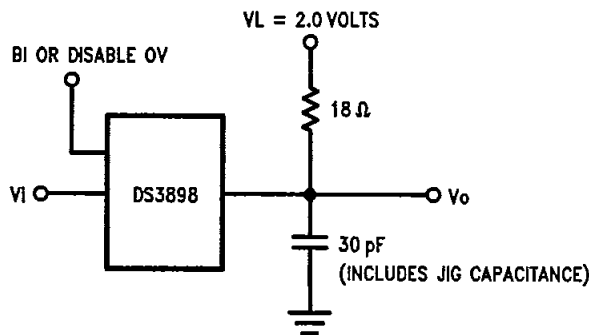
Note: $t_R = t_F < 2$ ns from 10% to 90%

TL/F/8700-11

FIGURE 4
Receiver Noise Immunity:
"No Response at Output" Input Waveforms



TL/F/8700-12



Note: $t_R = t_F < 10$ ns from 10% to 90%

TL/F/8700-13

FIGURE 5
Repeater Propagation Delays